REMARKS/ARGUMENTS

Claims 1-3, 5-39, 41 and 49-54 are in the present application. Claims 1, 3, 14, 18, 19, 22, 37, 38, 41 and 49 have been amended herein. Claims 42, 46 and 48 have been canceled without prejudice. New claims 52-54 have been added herein. Applicants request reconsideration and allowance of claims 1-3, 5-39, 41 and 49-51. Applicants further request consideration on the merit and allowance of claims 52-54.

Applicants thank the Examiner for the time and courtesy extended to applicants' attorney (Jun-Young Jeon, Reg. No. 43,693) during the telephone conference of March 24, 2005, during which the Advisory Action of March 24, 2005 was discussed.

I. "Response to Arguments" in the March 24, 2005 Advisory Action.

A. The term "integrated circuit chip" in the preamble

As discussed with the Examiner on March 24, 2005, the term "integrated circuit chip" has been more clearly incorporated into the body of claims 1, 22 and 41.

B. "Northbridge integrated circuit chip that transports MPEG video data"

Claim 22 has been amended to recite, in a relevant portion, "an MPEG video decoder for decoding MPEG video data to generate video for displaying is implemented on the integrated circuit chip." Since this integrated circuit chip is the one on which

the system bridge controller having a north bridge function is also implemented, it is more clear now that such an integrated circuit chip would not read on a mere Northbridge chip that may transport data including MPEG video data.

C. Articles cited by the Examiner

The article entitled "Desktop PC-IC Content and Integration Trends" by Scott Hudson ("Hudson article") recites "graphics can be integrated into the northbridge of the core logic chip set . . ." Applicants submit that this does not teach or suggest implementing an MPEG video decoder and a system bridge controller having a northbridge function on a single integrated circuit chip. Further, Applicants do not see any other more relevant section in the Hudson article.

The article entitled "Basic Notebooks Infrastructure in Place - Trident introduces Monterey chip; Neomagic re-engineering products" by Peter Brown ("Brown article") recites, in a relevant portion, ". . . the Monterey, an integrated graphics chip that combines 3-D core technology with the Northbridge core logic." Applicants submit that this also does not teach or suggest implementing an MPEG video decoder and a system bridge controller having a northbridge function on a single integrated circuit chip. Further, Applicants do not see any other more relevant section in the Brown article.

As such, neither of the articles newly discovered by the Examiner teaches or suggests implementing an MPEG video decoder with a system bridge controller having a north bridge function on the same integrated circuit chip.

II. Rejection of Claims 1-3, 5-39, 41-42, 46, and 48-51 under 35 U.S.C. § 102(e) in the August 11, 2004 Office Action

Claims 1-3, 5-39, 41-42, 46, and 48-51 have been rejected under 35 U.S.C. § 102(e) as allegedly being unpatentable over U.S. Patent No. 5,883,670 ("Sporer et al."). Since claims 42, 46 and 48 have been canceled herein, their rejection is now moot.

A. Rejection of Claim 1

In rejecting claim 1, the Office Action states "Sporer teaches a system on an integrated circuit chip comprising an MPEG video decoder for processing MPEG video data to generate video for displaying . . . (col. 10, lines 1-29; figs. 1 and 9), a system bridge controller for coupling a CPU to a plurality of peripheral devices (figs. 1 and 3), wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip (col. 3, line 54 to col. 4, line 28) . . . "

Claim 1 has been amended in view of the Advisory Action. Claim 1 now recites, in a relevant portion, "an MPEG video decoder for decoding MPEG video data to generate video for displaying; and a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to the plurality of peripheral devices, wherein the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip."

Sporer et al. does not teach or even suggest such a system "wherein the MPEG video decoder and the system bridge controller

are implemented on the single integrated circuit chip." By way of example, the PCI Bridge 34 in FIG. 1 of Sporer et al. is clearly external to the video processing circuit 22. In the August 11, 2004 Office Action, the controller 50 in FIG. 1 of Sporer et al. appears to be equated with a system bridge controller of the present invention. However, neither FIG. 1 nor FIG. 5 (which shows a detailed view of the controller 50) of Sporer et al. provides any indication that the controller 50 indeed has a north bridge function. In fact, the controller 50 requires an external PCI bridge (i.e., the PCI Bridge 34) to interface with the PCI Bus 36. If anything, Sporer et al. teaches away from the present invention by disclosing the use of an external PCI bridge, which results in an increased number of chips as well as providing an additional potential source of system failure.

Since Sporer et al. does not disclose all of the features of claim 1, claim 1 is not anticipated by Sporer et al. Further, the Hudson and Brown articles also fail to teach or suggest any such implementation of MPEG video decoder and a system bridge controller on a single integrated circuit chip. Therefore, applicants request that the rejection of claim 1 be withdrawn and that it be allowed.

B. Rejection of Claims 22 and 41

Further, for similar reasons as claim 1 discussed above, Sporer et al. does not disclose "coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function implemented on an integrated circuit chip, wherein an MPEG video decoder for decoding MPEG video data to

generate video for displaying is implemented on the integrated circuit chip" as in claim 22 of the present application, or "[a] system on a single integrated circuit chip comprising: an MPEG Transport processor . . . an MPEG video decoder . . . and a system bridge controller . . . wherein the MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip" as in claim 41; therefore, Sporer et al. does not anticipate claims 22 and 41.

Further, Hudson and Brown articles also do not teach or suggest such implementation of an MPEG Transport processor and/or an MPEG video decoder on the same integrated circuit chip as a system bridge controller. Therefore, applicants request that the rejection of claims 22 and 41 be withdrawn and that they be allowed.

C. Rejection of Claim 2-3, 14, 18-19, 23, 25, and 49

In rejecting claims 2-3, 14, 18-19, 23, 25, and 49, the Office Action states "Sporer discloses the system bridge controller is capable of performing format conversion between big-endian data and little endian data, between the CPU and one or more of the plurality of peripheral devices, between the CPU and at least one of the MPEG video decoder, the means for displaying the video and the other components for processing video and graphics," and cites FIGs. 1-3.

First of all, applicants do not see how "performing format conversion between big-endian and little endian data" is disclosed in FIGs. 1-3. Hence, if the rejection of claims 2, 3,

18, 23, 25 and 49[1] is to be maintained, applicants request some guidance from the Examiner as to the grounds for rejection of these claims.

Since claims 2-3, 14, 18-19, 23, 25, and 49 depend, directly or indirectly, from claims 1, 22 and 41, respectively, they incorporate all the terms and limitations of claim 1, 22 or 41 from which they depend in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 2-3, 14, 18-19, 23, 25, and 49 be withdrawn and that they be allowed.

D. Rejection of Claims 5 and 26

In rejecting claims 5 and 26, the Office Action states "Sporer discloses plurality of peripheral devices include one or more PCI devices, and wherein the system bridge controller includes a PCI bridge for coupling the CPU to the one or more PCI devices," and cites Col. 7, line 58 to Col. 8, lines 41 of Sporer et al.

As discussed above, Sporer et al. in FIG. 1 unequivocally teaches using the PCI Bridge 34 that is external to the video processing circuit 22. Therefore, Sporer et al. cannot possibly anticipate "a system . . . wherein the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip" wherein the system bridge controller includes a PCI bridge, or "a method . . . wherein an MPEG video decoder for decoding MPEG video data to generate video for

[1] Applicants note that claim 14 does not have such "format conversion" limitation.

displaying is implemented on the integrated circuit chip [as the system bridge controller having a northbridge function]" including "coupling the CPU to one or more PCI devices."

Further, since claims 5 and 26 depend from claims 1 and 22, respectively, they incorporate all the terms and limitations of claim 1 or 22 from which they depend in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 5 and 26 be withdrawn and that they be allowed.

E. Rejection of Claims 6, 10, 27 and 31

In rejecting claims 6, 10, 27 and 31, the Office Action states "Sporer discloses the PCI bridge is capable of performing a DMA function between the one or more PCI devices and an external memory." As these claims depend, directly or indirectly, from claims 1 and 22, respectively, they incorporate all the terms and limitations of claim 1 or 22 from which they depend, in addition to other limitations which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 6, 10, 27 and 31 be withdrawn and that they be allowed.

F. Rejection of Claims 7-8, 12-13, 28-29, 33-34, and 37-38

The Office Action states "Sporer discloses PCI bridge is capable of performing format conversion between big/little endian data used in the CPU and little/big endian data used in the one or more PCI devices," and cites col. 1, line 52 to col. 2, line 9 and col. 7, line 58 to col. 10, line 67. After having

reviewed this vast range of text in the specification, applicants do not see any disclosure of such big/little endian format conversion. Hence, if the rejection of these claims is to be maintained, applicants respectfully request some guidance from the Examiner as to the grounds for rejection of these claims.

Further, since claims 7-8, 12-13, 28-29, 33-34 and 37-38 depend, directly or indirectly, from claims 1 and 22, respectively, they incorporate all the terms and limitations of claim 1 or 22 from which they depend, in addition to other limitations which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 7-8, 12-13, 28-29, 33-34 and 37-38 be withdrawn and that they be allowed.

G. Rejection of Claims 9, 11, 16, 17, 30, 32, 35, 36 and 50-51

Claims 9, 11, 16, 17, 30, 32, 35, 36 and 50-51 have been rejected on various different grounds as allegedly being anticipated by Sporer et al. Since claims 9, 11, 16, 17, 30, 32, 35, 36 and 50-51 depend, directly or indirectly, from claims 1, 22 and 41, respectively, they incorporate all the terms and limitations of claim 1, 22 or 41, in addition to other limitations which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 9, 11, 16, 17, 30, 32, 35, 36 and 50-51 be withdrawn and that they be allowed.

H. Rejection of Claims 15, 20-21, 24, 39, 42, 46 and 48

Claims 15, 20-21, 24, 39, 42, 46 and 48 appear to have been rejected based on the same or similar grounds as claims 1, 22 and 41, respectively. Since claims 42, 46 and 48 have been canceled herein, their rejection is now moot. Since claims 15, 20-21, 24 and 39 depend from claims 1 and 22, respectively, they incorporate all the terms and limitations of claim 1 or 22 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 15, 20-21, 24 and 39 be withdrawn and that they be allowed.

I. New Claims 52-54

Claim 52 recites, in a relevant portion, "an MPEG Transport processor implemented on the single integrated chip." None of the cited references teaches or suggests the implementation of an MPEG Transport processor on the same integrated circuit chip as an MPEG video decoder and a system bridge controller having a north bridge function.

Claim 53 recites, in a relevant portion, "a video compositor implemented on the single integrated circuit chip, wherein the video compositor blends the video generated by the MPEG video decoder with graphics." None of the cited references teaches or suggests the implementation of a video compositor on the same integrated circuit chip as an MPEG video decoder and a system bridge controller having a north bridge function.

Claim 54 depends from claim 53, and further recites, "a graphics blender implemented on the single integrated circuit chip, wherein the graphics blender blends two or more graphics

windows to generate the graphics provided to the video compositor." None of the cited references teaches or suggests the implementation of a graphics blender and the video compositor on the same integrated circuit chip as an MPEG video decoder and a system bridge controller having a north bridge function.

Further, since new claims 52-54 depend, directly or indirectly, from claim 1, they incorporate all the terms and limitations of claim 4 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that claims 52-54 be allowed.

III. Concluding Remarks

In view of the foregoing amendments and remarks, applicants respectfully request an early issuance of a patent with claims 1-3, 5-39, 41 and 49-54. If there are any remaining issues that can be addressed over the telephone, the Examiner is invited to call applicants' attorney at the number listed below.

Respectfully submitted,
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